

MCA.I/02.22.003

Reg. No

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MCA DEGREE FIRST SEMESTER EXAMINATION, FEBRUARY 2022
20-382-0103 DIGITAL ELECTRONICS AND COMPUTER ORGANIZATION
(Regular)

Time : 3 Hours

Maximum Marks:50

Write any five questions.
(Each question carries 10 Marks)

Q.NOS	QUESTIONS	MARKS	CO	BL	PI
1.	(a) Simplify the following expressions, and implement them with two-level NAND gate circuits: $AB' + ABD + ABD' + A'C'D' + A'BC'$	5	CO3	L3	1.7.1
	(b) Convert the following: (i) If $N^2 = (6100)_8$ then find out the value of N (ii) Find out $(DE)_{16} - (88)_{16}$	5			
2.	(a) Illustrate the implementation of subroutine with example.	5	CO4	L4	2.5.2
	(b) Illustrate the implementation of different addressing modes to find out the sum of N numbers using assembly language.	5	CO2	L2	1.7.1
3.	(a) Explain direct and associative mapping with reference to cache memory.	6	CO5	L2	1.7.1
	(b) Consider a direct mapped cache of size 64 KB with block size 512 bytes. The size of main memory is 4GB. Find Number of bits in tag.	4			

4.		Illustrate Branch delay and Memory delay with example.	10	CO5	L4	1.7.1							
5.	(a)	Write down the sequence of actions needed to fetch and execute the instruction, Branch_if_[R2]=[R3] LOOP.	4	CO5	L2	2.5.3							
	(b)	<p>A 5-stage pipelined processor has Instruction Fetch (IF), Instruction Decode (ID), Operand Fetch (OF), Perform Operation (PO) and Write Operand (WO) stages. The IF, ID, OF and WO stages take 1 clock cycle each for any instruction. The PO stage takes 1 clock cycle for ADD and SUB instructions, 2 clock cycles for MUL instruction, and 5 clock cycles for DIV instruction respectively. Operand forwarding is used in the pipeline. What is the number of clock cycles needed to execute the following sequence of instructions?</p> <table><tr><th>Instruction</th><th>Meaning of instruction</th></tr><tr><td>I0 :MUL R2 ,R0 ,R1</td><td>$R2 \leftarrow R0 * R1$</td></tr><tr><td>I1 :DIV R5 ,R3 ,R4</td><td>$R5 \leftarrow R3 / R4$</td></tr><tr><td>I2 : ADD R2 ,R5 ,R2</td><td>$R2 \leftarrow R5 + R2$</td></tr><tr><td>I3 :SUB R5 ,R2 ,R6</td><td>$R5 \leftarrow R2 - R6$</td></tr></table>	Instruction				Meaning of instruction	I0 :MUL R2 ,R0 ,R1	$R2 \leftarrow R0 * R1$	I1 :DIV R5 ,R3 ,R4	$R5 \leftarrow R3 / R4$	I2 : ADD R2 ,R5 ,R2	$R2 \leftarrow R5 + R2$
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I2 : ADD R2 ,R5 ,R2	$R2 \leftarrow R5 + R2$												
I3 :SUB R5 ,R2 ,R6	$R5 \leftarrow R2 - R6$												
6.	(a)	Convert the octal number 540 to binary number	2	CO2	L2	1.7.1							
	(b)	Express +39 and -39 in 1's compliment and 2's compliment form.	3										
	(c)	Convert the decimal fraction 2550. 312510 to Binary number.	2.5										
	(d)	Convert (5AC2) ₁₆ to Decimal Number.	2.5										
7.	(a)	State the Booth's algorithm for multiplication of two numbers.	4	CO6	L2	1.7.1							
	(b)	Perform Multiplication on the numbers 15 and -13 using Booth's Algorithm.	6										
